

This Page Is Inserted by IFW Operations  
and is not a part of the Official Record

## **BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

**IMAGES ARE BEST AVAILABLE COPY.**

**As rescanning documents *will not* correct images,  
please do not report the images to the  
Image Problem Mailbox.**

1/3

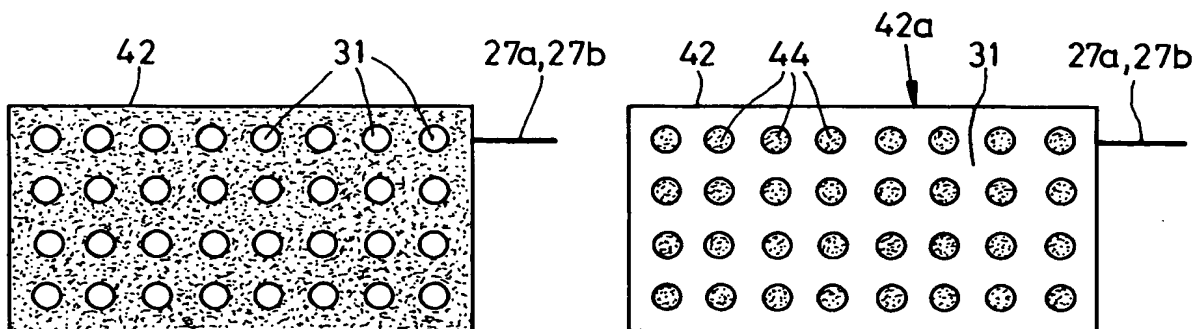
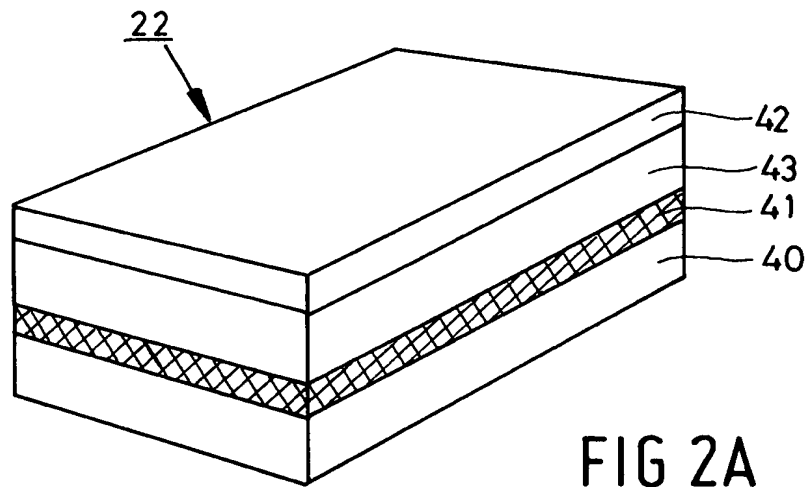
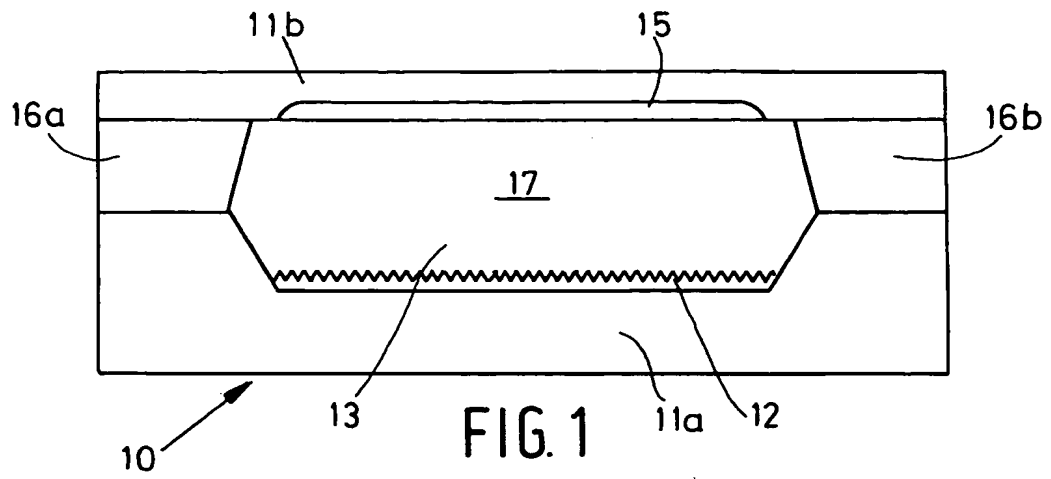
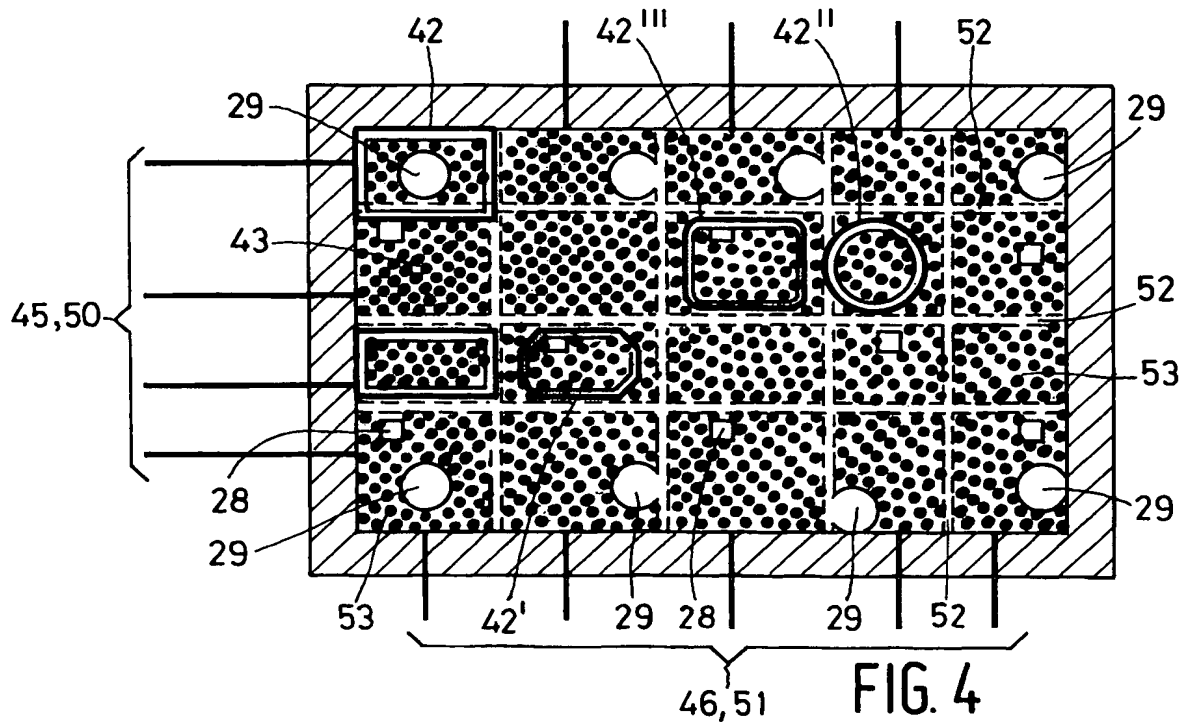
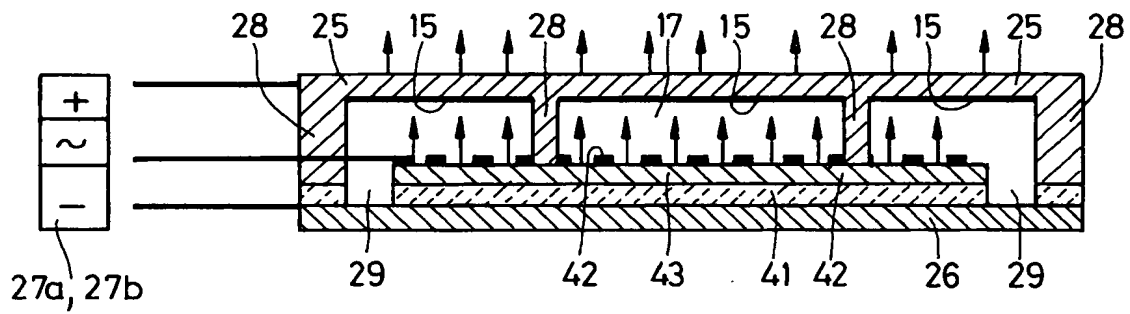
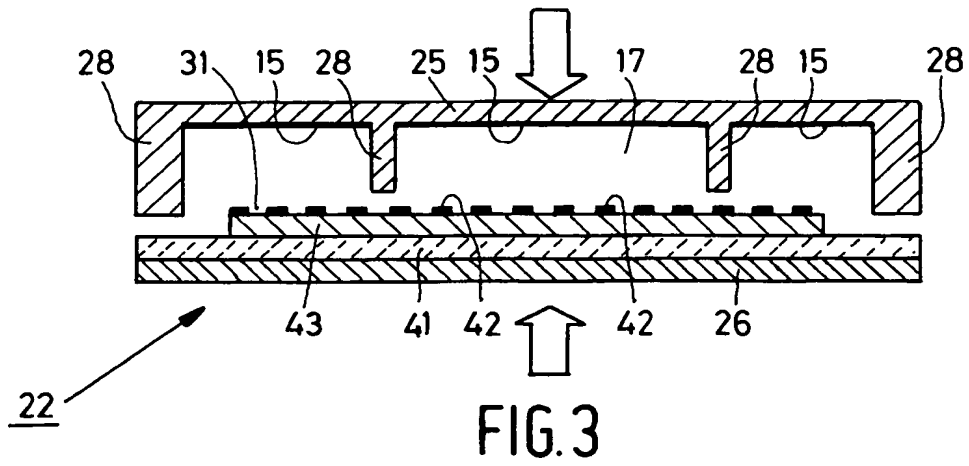


FIG. 2B

FIG. 2C

2/3



A block diagram illustrating a system architecture. A central component labeled "MUX" (multiplexer) receives input from a block labeled "61" via a thick arrow. The MUX has multiple output lines labeled "45-46" that connect to a large, rounded rectangular component labeled "66". This component "66" contains internal elements labeled "67" and "15". Below the MUX, there are two more blocks: "62" and "63". Block "62" sends an upward signal labeled "27a-27b" to the MUX. Block "63" sends a downward signal to a block labeled "64". Block "64" then sends signals upwards, labeled "65a", "65a'", "65b", and "65b'". Additionally, there are labels "65c" and "65c'" near the bottom right of the main assembly.

FIG. 6